REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed November 1, 2007. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 1-20 and 22-35 are pending in the present application. Claims 1-20 and 22-35 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Arnold et al (U.S. Pat. No. 6,438,681, hereinafter "Arnold"). Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Response to Claim Rejections Under 35 U.S.C. § 102

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102.

Claims 1-20 and 22-35 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Arnold. For at least the reasons set forth below, Applicants traverse these rejections.

Claims 1-18

Applicants respectfully submit that independent claim 1 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the features emphasized below in claim 1.

Independent claim 1, as amended, recites (emphasis added):

> 1. A method of monitoring and controlling instruction dependency for microprocessors, the method comprising:
> fetching an instruction at one or more thread control elements from an instruction buffer;
> comparing, with a comparator, one or more source operand identifications of the instruction to one or more temporary register identifications,
> ***comparing, with the comparator, a thread control ID associated with the thread control element with pipeline thread control IDs in a pipeline***,
> wherein each thread control element and comparator forms a bi-directional correspondence, and wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations;
> verifying whether any of the one or more source operand identifications at the thread control element matches any of the one or more temporary register identifications and ***verifying whether the thread control ID matches any pipeline thread control IDs***; and
> ***in response to a match between the source operand identification and the temporary register identification and a match between the thread control ID and a pipeline thread control ID***, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle, wherein the match corresponds to instruction dependency.

In an effort to advance prosecution of the application, Applicants have amended claim 1 to further define the claimed embodiment and submit that no new matter is added by the amendment. Applicants respectfully submit that the Arnold reference fails to teach the feature emphasized above. In particular, Arnold fails to teach of "comparing, with the comparator, a thread control ID associated with the thread control

element with pipeline thread control IDs in a pipeline." After acquiring an instruction data stream from the instruction buffer (101), a thread control element sends the source operand ID's of the acquired instruction data stream along with a thread control ID to a comparator corresponding to the thread control element. Applicants submit that the Arnold reference fails to teach this step. At most, Arnold teaches the following:

> The n-bit register identifier in each stage 25, 28, 32, and 35 is transmitted to comparison logic 24, which is configured to compare the register identifiers to determine whether a data dependency that defines a data dependency hazard exists between any of the instructions associated with the n-bit register identifiers.

(Col. 6, lines 50-55). While Arnold teaches of comparing register identifiers, Arnold fails to disclose, teach, or suggest comparing each source operand ID of the one or more source operand IDs and the thread control ID to each of the temporary register ID/thread control ID pairs contained in the temporary register ID/thread control ID pipelines unit. As such, Arnold also fails to teach the limitation, "in response to a match between the source operand identification and the temporary register identification and a match between the thread control ID and a pipeline thread control ID . . ."

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the highlighted features in claim 1 above. Furthermore, Applicants submit that dependent claims 2-18 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988). Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, these dependent claims recite further features/steps and/or combinations of

features/steps, as apparent by examination of the claims themselves, that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable.

Claims 19-28

Applicants respectfully submit that independent claim 19 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the features emphasized below in claim 19.

Independent claim 19 recites (emphasis added):

> 19. A method of monitoring and controlling instruction dependency for microprocessor systems, the method comprising:
> a) fetching an instruction at a thread control element;
> b) receiving an instruction request at an arbiter, wherein the instruction request is issued from the thread control element;
> c) comparing one or more source operand identifications of the instruction at the thread control element to one or more temporary register identifications and ***comparing a thread control ID associated with the thread control element with pipeline thread control IDs in a pipeline***, wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations, and ***wherein said one or more source operand instructions at said thread control element is not part of a pipeline or pipelines***;
> d) verifying whether any of the one or more source operand identifications matches any of the one or more temporary register identifications ***and verifying whether the thread control ID matches a pipeline thread control ID***;
> e) in response to a match of the source operand identification and the temporary register identification ***and a match between the thread control ID and the pipeline thread control ID***, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle, wherein the match corresponds to instruction dependency;
> f) if none of the one or more source operand identifications matches any of the one or more temporary register identifications:

f1) verifying whether a destination operand of the instruction is a temporary register; and

f2) if the destination operand of the instruction is a temporary register:

writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipeline storage locations;

f3) if the destination operand of the instruction is not a temporary register: writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations.

In the Response to Arguments section, the Examiner rejects Applicants' argument that Arnold does not disclose a thread control element outside of a pipeline stage or storage location. In particular, the Examiner asserts that "*the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)*" (Office Action, page 14). (The Examiner relies on this reasoning in rejecting claim 19.) However, Applicants respectfully disagree. With reference to FIG. 3 (reproduced below), Arnold clearly depicts latches 89, 91, and 93 in addition to processing circuitry 66 as part of the pipeline 21.

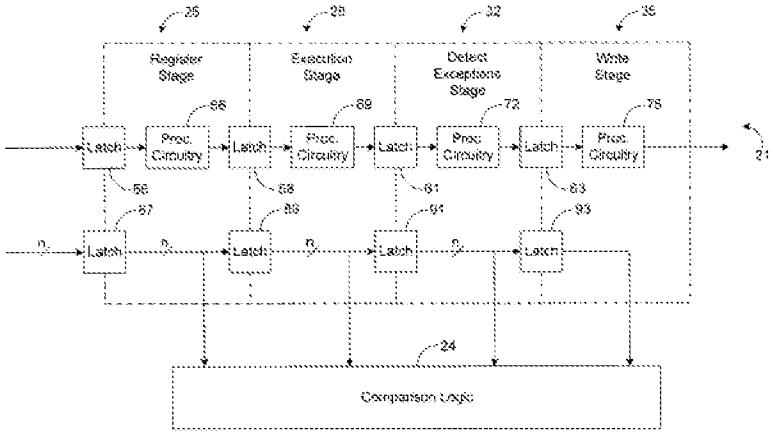

FIG. 3
(Prior Art)

In fact, Arnold states that "pipelines 21 typically process instructions in stages" and "[t]he pipelines 21 shown by FIG. 1 process the instructions in four stages: a register stage 25, an execution stage 28, a detect exceptions stage 32, and a write stage 35." (Col. 3, lines 33-40) and "the n-bit register identifier is latched into stages 25, 28, 32, and 35 by latches 87, 89, 91, and 93, respectively, on the same edges that the instruction is respectively latched into stages 25, 28, 32, and 35." (Col. 3, lines 33-40; col. 6, lines 42-46). Applicants respectfully submit that the Examiner improperly attempts to partition the register stage 25 and corresponding processing circuitry 66 from the rest of the pipeline 21 in rejecting claim 19. Arnold does not explicitly state that the processing circuitry 66 is not part of the pipeline 21. Furthermore, Applicants note that the Office Action alleges that "*the register stage circuitry is outside of the temporary register identification pipeline storage locations.*" However, claim 19 does not recite this, but instead recites: "wherein said one or more source operand instructions at said thread control element is not part of a pipeline or pipelines." This feature refers to the actual source operands. As depicted in FIG. 5 of Arnold, the instruction dispersal unit 18 feeds directly into the pipeline 132. ("[T]he processing system 15 includes an instruction dispersal unit 18 that receives instructions of a computer program and assigns each instruction to one of a plurality of pipelines 21.")

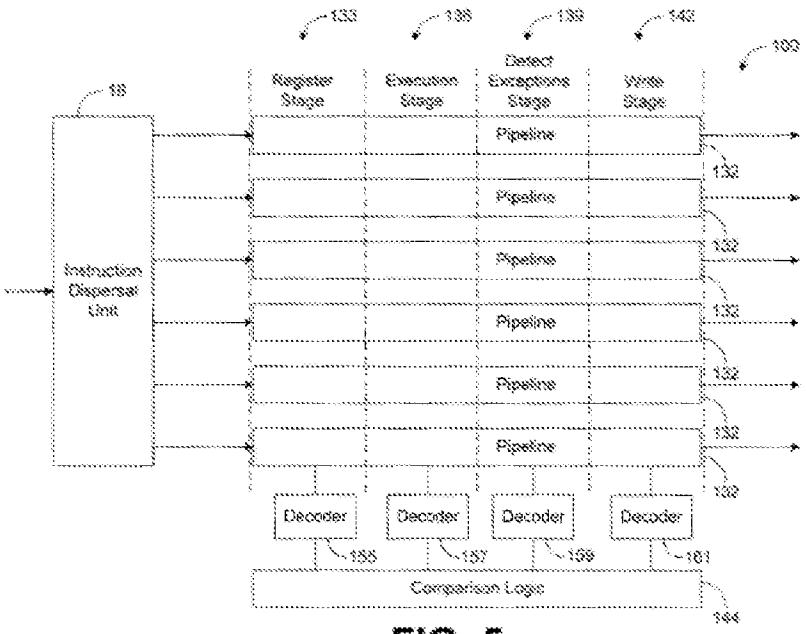

FIG. 5

As such, Arnold apparently fails to teach the limitation, "wherein said one or more source operand instructions at said thread control element is not part of a pipeline or pipelines." For at least this reason, Applicants respectfully submit that independent claim 19 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the highlighted features in claim 19 above.

Notwithstanding, Applicants have amended claim 19 to further emphasize certain novel features of the claimed embodiment. No new matter is added by the amendments. Applicants respectfully submit that the Arnold reference fails to teach the other features emphasized above in claim 19. For at least the foregoing reasons, independent claim 19 patently defines over Arnold.

Applicants submit that dependent claims 20-28 are allowable for at least the reason that these claims depend from an allowable independent claim. Additionally and notwithstanding the foregoing reasons for the allowability of claim 19, these dependent claims recite further features/steps and/or combinations of features/steps, as

apparent by examination of the claims themselves, that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable.

Claims 29-34

Applicants respectfully submit that independent claim 29 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the features emphasized below in claim 29.

Independent claim 29 recites (emphasis added):

> 29. A system for instruction dependency monitor and control, comprising:
> a set of one or more thread control elements for fetching instructions, ***wherein said thread control elements are not part of a pipeline stage or pipeline storage location***;
> a set of one or more comparing elements, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements; and
> a set of one or more temporary register identification pipeline storage locations, wherein the one or more temporary register identification pipeline storage locations are directly coupled to the one or more comparing elements.

In alleging that Arnold teaches the feature emphasized above in claim 29, the Office Action relies on substantially the same reasoning used to reject claim 19 above. First, the Office Action apparently equates "thread control elements" with register stage 25 (and specifically, to "register stage processing circuitry"). Based on this reasoning, the Office Action then again asserts that "*the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)*" (Office Action, pages 10-11). Applicants disagree and

respectfully submit that Arnold clearly depicts latches 89, 91, and 93 in addition to processing circuitry 66 as part of the pipeline 21. Arnold states that "pipelines 21 typically process instructions in stages" and "[t]he pipelines 21 shown by FIG. 1 process the instructions in four stages: a register stage 25, an execution stage 28, a detect exceptions stage 32, and a write stage 35." (Col. 3, lines 33-40). Moreover, Arnold teaches that "the n-bit register identifier is latched into stages 25, 28, 32, and 35 by latches 87, 89, 91, and 93, respectively, on the same edges that the instruction is respectively latched into stages 25, 28, 32, and 35." (Col. 6, lines 42-46). Applicants respectfully submit that the Examiner improperly attempts to partition the register stage 25 and processing circuitry 66 from the rest of the pipeline 21.

Accordingly, Applicants respectfully submit that independent claim 29 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the highlighted features in claim 29 above. Furthermore, Applicants submit that dependent claims 30-34 are allowable for at least the reason that these claims depend from an allowable independent claim.

Additionally and notwithstanding the foregoing reasons for the allowability of claim 29, these dependent claims recite further features/steps and/or combinations of features/steps, as apparent by examination of the claims themselves, that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable.

Claim 35

Applicants respectfully submit that independent claim 35 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the features emphasized below in claim 35.

Independent claim 35 recites (emphasis added):

> 35. A system for instruction dependency monitor and control, comprising:
> ***a set of one or more thread control elements for fetching instructions wherein said thread control elements are not part of a pipeline stage or storage location***;
> a set of one or more comparing elements, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements and wherein each thread control element and comparing element forms a bi-directional correspondence;
> a set of one or more temporary register identification pipeline storage locations, wherein the one or more temporary register pipeline storage locations are directly coupled to the one or more comparing elements, and
> an arbiter coupled to the thread control elements, the comparing elements, and the temporary register pipeline storage locations in each stage of a pipeline or pipelines.

In alleging that Arnold teaches the feature emphasized above in claim 35, the Office Action relies on substantially the same reasoning used to reject claim 29 above. First, the Office Action apparently equates "thread control elements" with register stage 25 (and specifically, to "register stage processing circuitry"). Based on this reasoning, the Office Action then again asserts that "*the register stage circuitry is outside of the temporary register identification pipeline storage locations (comprising latches 89, 91, and 93; See FIG. 3)*" (Office Action, page 12). Applicants disagree and respectfully submit that Arnold clearly depicts latches 89, 91, and 93 in addition to processing circuitry 66 as part of the pipeline 21. Arnold states that "pipelines 21 typically process instructions in stages" and "[t]he pipelines 21 shown by FIG. 1 process the instructions

in four stages: a register stage 25, an execution stage 28, a detect exceptions stage 32, and a write stage 35." (Col. 3, lines 33-40). Arnold also teaches that "the n-bit register identifier is latched into stages 25, 28, 32, and 35 by latches 87, 89, 91, and 93, respectively, on the same edges that the instruction is respectively latched into stages 25, 28, 32, and 35." (Col. 6, lines 42-46). Applicants respectfully submit that the Examiner improperly attempts to partition the register stage 25 and corresponding processing circuitry 66 from the rest of the pipeline 21. Accordingly, Applicants respectfully submit that independent claim 35 patently defines over Arnold for at least the reason that Arnold fails to disclose, teach or suggest the highlighted features in claim 35 above.

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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